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Dawoud, D.S.;
Communications and Signal Processing, 1997. COMSIG '97., Proceedings of the 1997 Symposium on
9-10 Sept. 1997 Page(s):173 - 178

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☐ 2. **Digit-serial fixed coefficient complex number multiplier-accumulator on FPGAs**
Sansaloni, T.; Valls, J.; Parhi, K.K.;
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International
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☐ 3. **A generalized multibit recoding of two's complement binary numbers and its pro application in multiplier implementations**
Sam, H.; Gupta, A.;
Computers, IEEE Transactions on
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☐ 4. **Comparison of constant coefficient multipliers for CSD and Booth recoding**
Hu, A.; Al-Khalili, A.J.;
Microelectronics, The 14th International Conference on 2002 - ICM
11-13 Dec. 2002 Page(s):66 - 69

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☐ 5. **A new architecture of matched-filter employing coefficient recode technique for communication systems**
Xiaoxu Guo; Jie Chen; Yulin Qui;
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Volume 2, 21-24 Oct. 2003 Page(s):800 - 803 Vol.2

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☐ 6.
On complexity reduction of FIR digital filters using constrained least squares sol
Muhammad, K.; Roy, K.;
Computer Design: VLSI in Computers and Processors, 1997. ICCD '97. Proceedings.,